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Electrical Contact at the Interface between Silicon and Transfer-Printed Gold Films by Eutectic Joining

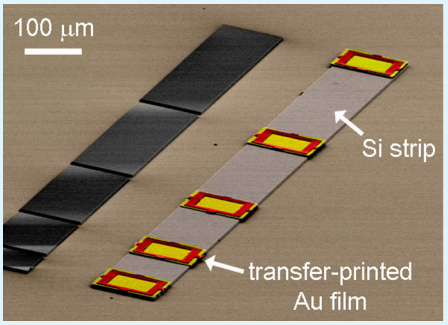
Hohyun Keum,[†] Hyun-Joong Chung,[‡] and Seok Kim*,[†]

[†]Department of Mechanical Science and Engineering, University of Illinois at Urbana−Champaign, Urbana, Illinois 61801, United States

[‡]Department of Chemical and Materials Engineering, University of Alberta, Edmonton, Alberta T6G 2V4, Canada

Supporting Information

ABSTRACT: This paper presents the electrical and morphological properties at the interface between a metal (Au) and a semiconductor (Si) formed by a novel transfer-printing technology. This work shows that a transfer-printed thin (hundreds of nanometers) Au film forms excellent electrical contact on a Si substrate when appropriate thermal treatment is applied. The successful electrical contact is attributed to eutectic joining, which allows for the right amount of atomic level mass transport between Au and Si. The outcomes suggest that transfer-printing-based micromanufacturing can realize not only strong mechanical bonding but also high-quality electrical contact via eutectic joining.



KEYWORDS: *transfer printing, contact resistance, transmission line model, eutectic bonding, metal−semiconductor contact*

INTRODUCTION

Transfer printing involves the use of a soft stamp to transfer solid micro/nanoscale materials from a substrate where they are generated or grown to a different substrate for device integration.[1−4] This technique has been emerging because of its attractive capabilities of heterogeneous material integration[5−9] and assembly of common electronic devices on soft substrates to fabricate flexible electronics.[10−15] Besides, transfer printing has been explored to manufacture microsystems particularly when combined with direct-bonding techniques such as silicon fusion bonding via annealing.[16] The transfer-printing-based micromanufacturing (termed "micromasonry")[16] enables the three-dimensional adhesiveless deterministic assembly of homogeneous as well as heterogeneous materials at microscale. Because of the adhesiveless assembly capabilities, it has the potential to impact numerous vital microsystems that cannot easily be accommodated with other existing methods.[16−18] In spite of its capability to create enormous applications, many scientific and technological aspects of transfer-printing-based micromanufacturing have not yet been explored. For example, the thermal conductance at the interface between a transfer-printed gold (Au) film and a smooth silicon (Si) substrate was recently investigated and turned out to be only a factor of 3 smaller than that of the corresponding interface formed by vacuum deposition.[19] Other interfacial properties that are important but have not yet been explored include optical and electrical contacts.

Here, we present an electrical contact resistance of the interface between gold (Au) thin films and silicon (Si) assembled via transfer printing. We transfer-printed Au films onto a Si substrate to make a sample and annealed the sample at different temperatures for different time durations to modulate the contact resistance between Au and Si. A transmission line model (TLM) was employed to measure the contact resistance of the samples. The collected data were compared with the contact resistance for a counterpart interface between sputtered Au with a chromium (Cr) adhesive layer and Si, which is commonly used in microfabrication. Our experimental results reveal that the contact resistance of transfer-printed Au films and Si is comparable to the contact resistance of its vacuum-deposited counterpart when appropriate thermal treatment is followed. Specifically, annealing at a temperature slightly above the bulk eutectic (~360 °C) for less than 30 min provides excellent electrical contact with smooth Au film morphology. Annealing for a longer time and/or at higher temperature causes a rupture in the Au film. Annealing at a temperature below the bulk eutectic results in a high electrical contact resistance. A comparison with the literature suggests that the quality of the electrical contact via transfer printing and subsequent annealing is nearly the same as the known values for the interface of vacuum-deposited Au and Si substrates (see the Supporting Information). This outcome proves that transfer-printing-based micromanufacturing, i.e., micromasonry, can develop the interface between assembled heterogeneous materials with significantly low electrical contact resistance.

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RESULTS AND DISCUSSION

Figure 1 demonstrates the schematic illustration of the transfer-printing procedure of 400 nm thick, 100 μm × 100 μm Au films

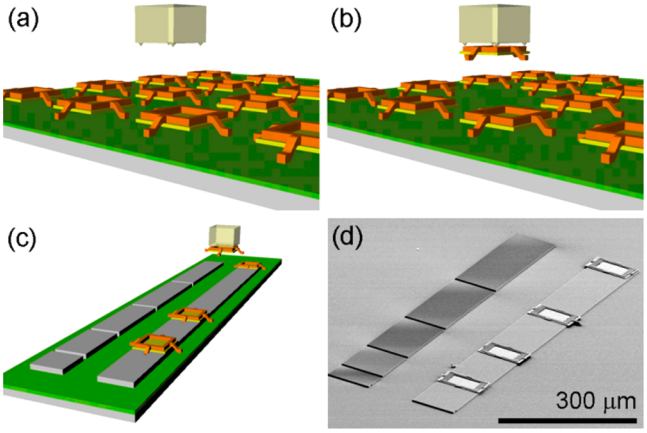

Figure 1. Schematic view of the fabrication procedure: (a) donor substrate with 400-nm-thick, 100 μm × 100 μm Au films; (b) retrieval of the film using an elastomeric stamp; (c) printing of the retrieved film on a Si strip with spacings of 200, 300, and 400 μm; (d) SEM image of a fully fabricated Si strip with Au films and a neighboring patterned Si that was used as an alignment mark during transfer printing.

that are prepared on a donor substrate through the fabrication process developed elsewhere[19] (see the Supporting Information) and a scanning electron microscopy (SEM) image of Au films on a Si strip assembled via micromasonry. First, Au films with photoresist frames are retrieved from a donor substrate and printed on a highly doped (ρ = 0.001−0.006 Ω·cm) Si strip, which was patterned on the top of a SiO_2 layer of a receiver substrate. Adjacent to this Si strip are a set of patterned Si islands that were used as alignment marks during transfer printing. Next, the substrate with printed Au films and the Si strip were placed into a rapid thermal-annealing furnace and annealed at various temperatures for various durations to enhance the strength of the adhesion between the Au films and the Si strip. This annealing step completed the preparation of the sample of Au−Si for the following TLM measurement. In order to validate the electrical contact resistance for the prepared sample, a control sample was also prepared through conventional microfabrication. 400-nm-thick Au films with 2-nm-thick Cr adhesive layers were patterned on a Si strip through sputter deposition in the control sample.

A total of 12 samples with different annealing conditions in terms of temperature and duration are summarized in Figure 2a. For these samples, the surface morphology of the Au films and the electrical contact resistance of transfer-printed Au films and Si strips were characterized. Four distinctive categories were identified, which we denote as regimes A−D. The surface morphology of the samples was examined through SEM images. Figure 2b represents the surface morphology seen from Au films annealed with the conditions of regimes A and B. Here, the root-mean-square (RMS) roughness of the Au films was less than 10 nm, measured by atomic force microscopy (AFM) at a scan size of 20 × 20 μm^2. While the Au films in regimes A and B are not as smooth as the vacuum-deposited Au−Cr surface (RMS of 0.85 nm), they showed identically smooth and flat morphology without any significant alteration. As shown in Figure 2c, the surface became considerably

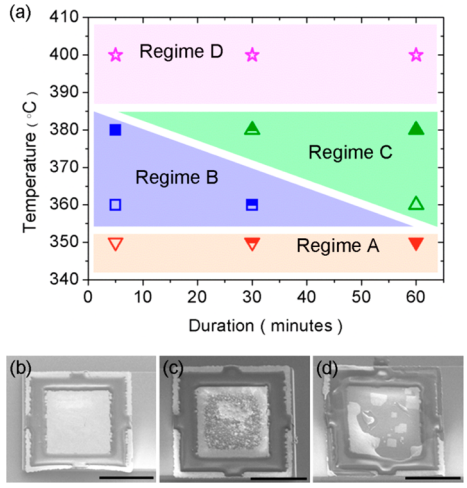

Figure 2. (a) Different regimes with different annealing conditions based on the morphology change and the electrical contact resistance of transfer-printed Au films, (b) the unaltered surface morphology for regimes A and B, (c) the roughened surface morphology for regime C, and (d) the ruptured surface morphology for regime D. All scale bars represent 50 μm.

roughened in regime C with RMS roughness of 50−70 nm. In spite of the surface roughness, the Au films in regime C completely covered the Si strip; thus, their functionality as metal contact pads on the semiconductor was still valid. However, Au films annealed at 400 °C in regime D exhibited undesirable ruptured surfaces (Figure 2d). In this regime, the bare Si surface is exposed; thus, the Au films cannot function as metal contact pads.

While the surface morphology indicates the structural validity of Au films as a metal pad on silicon, the quality of the electrical contact between the two different materials can be quantified by contact resistance. Contact resistances were collected by plotting current−voltage (I−V) curves using a probe station (4155c semiconductor parameter analyzer, Agilent). Between two adjacent Au films, a voltage bias from −0.1 to +0.1 V was applied and the current were simultaneously measured. From the obtained current and voltage values, the total resistance (R_T) between two Au films with various spacing was plotted in Figure 3. The total resistance consists of 2 times the interfacial contact resistance between the Au film and highly doped Si strip (R_C) and the access resistance, which is the sheet resistance of Si (R_{SH}) times the spacing between two probed Au films (d) divided by the width of the Au films (w). Assuming that R_C does not change when d is varied, the equation for R_T is[20−22]

$$R_T = 2R_C + \frac{R_{SH}d}{w} \quad (1)$$

From eq 1, the y intercept is 2 times the contact resistance between Si and Au and the slope represents the sheet resistance of the Si strip. Contact resistance (R_C) data obtained from linear regressions in Figure 3, where a fixed slope value from the sputter-deposited film is used, are summarized in Table 1. As can be seen from the table, regime A, where the samples are annealed below 360 °C or nonannealed, exhibits a much larger contact resistance than other samples annealed at or above 360 °C. A detailed description of the electrical properties in regime A is described in the Supporting Information. The contact resistance values for the samples annealed in regimes B and C

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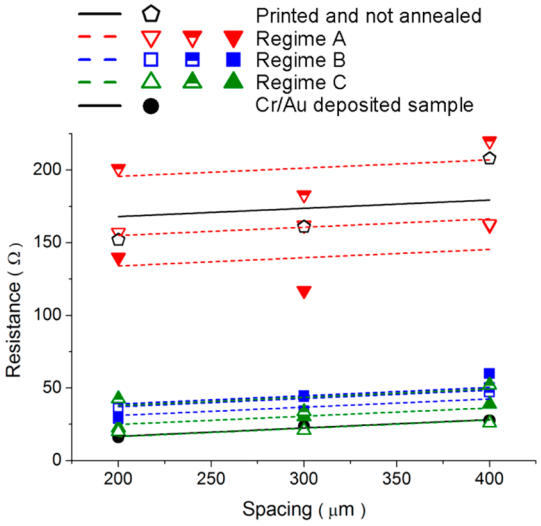

Figure 3. Plot of the total resistance versus spacing between two adjacent Au films. Different marks represent different annealing conditions, as described in Figure 2.

Table 1. Contact Resistance (R_C, Ω) Values from Figure 3[a]

	duration		
temperature (°C)	5 min	30 min	60 min
380	27.60	5.14	25.67
360	26.50	19.68	13.48
350	184.23[b]	126.23[b]	143.57[b]
sputtered Au/Cr	5.37		

[a]A fixed slope value (0.057 Ω/μm) was used for linear fitting. [b]R_C after the "burn-in" process (see the Supporting Information).

were remarkably small. They are only a factor of 1−5 larger than the contact resistance for Au films with Cr adhesive layers sputter-deposited on Si. The contact resistance of the samples in regime D was not measurable because Au films were ruptured during annealing.

A useful metal contact on a semiconductor requires a minimal loss of the electrical current at the interface between a metal and a semiconductor. In addition, it is preferred that the metal contact do not roughen to rupture or develop hillocks during the fabrication process. From a quick glance of Figure 3, one can postulate that an annealing temperature of 360 °C makes a sharp transition that divides "poor" (regime A) and "good" (regimes B and C) electrical contacts. However, a longer annealing time for temperatures at or above 360 °C can cause a roughening in the surface morphology, leading to a ruptured Au film in regime D. This rupture becomes instantaneous at or above 400 °C of annealing. In this study, regime B showed an optimized process window with reasonable electrical contact resistance and smooth Au film morphology. In order to understand the underlying mechanism that drives the electrical joining of the transfer-printed Au on Si, it is useful to revisit fundamental concepts from studies on the interface between vacuum-deposited Au and Si. Pure Si and Au exhibit high melting temperatures of ∼1060 and ∼1410 °C, respectively. However, alloying at the interface significantly decreases the melting temperature to as low as ∼360 °C at a composition ratio of 19 atom % of Si.[23] This is called eutectic melting. In addition to eutectic melting, interfacial mixing between Au and Si is known to take place at significantly lower temperature than the eutectic melting point, even at room temperature.[24−29] In our study, we observed Si diffusion into the Au film at all annealing temperatures (350−400 °C). Interface morphology after annealing can be directly visualized by AFM and SEM in Figure 4 by etching Au with an iodine-based wet etchant. Pits are the sites that Si atoms diffused out of the wafer. The reverse pyramidal shape in the (100) wafer stems from the anisotropic nature of Au−Si interaction, where the ⟨111⟩ plane has the highest atomic density, thus the slowest in losing the atoms.[30] It is notable that regimes A and B, where the electrical contact is poor and good, respectively, have qualitatively identical internal morphologies in parts b and d of Figure 4, respectively. The larger pits in Figure 4d can readily be understood as a kinetic effect that more Si atoms diffuse out at higher temperature (360 vs 350 °C) for longer time (60 vs 30 min).

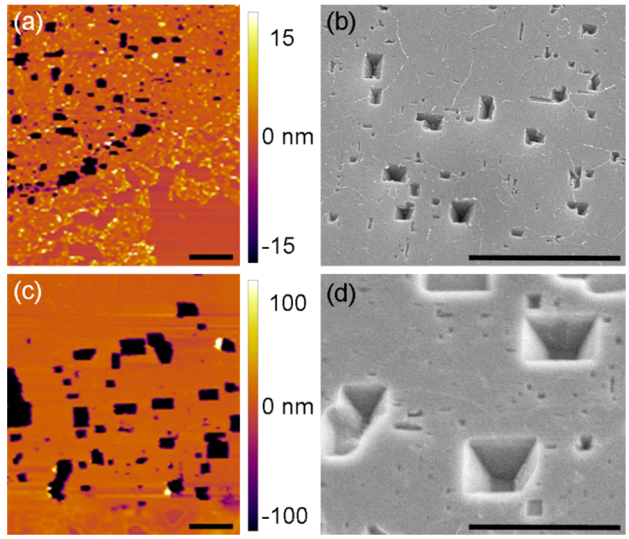

Figure 4. AFM and SEM images of Si strips after etching Au films: (a and b) annealing conditions of 350 °C for 30 min; (c and d) annealing conditions of 360 °C for 60 min. All scale bars represent 2 μm.

A rather striking feature is the sharp transition of the electrical contact at 360 °C for regimes A vs B and C. For example, annealing for 2 h at 350 °C leads to poor contact, whereas 5 min at 360 °C is sufficient to make a good contact (see the Supporting Information). However, the internal morphology in Figure 4 clearly suggests the intermixing of Au and Si at the interface for both temperatures. In fact, the poor electrical contact in spite of the interfacial Au−Si mixing was previously reported for 200 °C annealed Au coatings on the (100) Si wafer.[31] In order to reconcile the discrepancy between the electrical and morphological properties, we suggest two possible explanations. The first possibility is the formation of electrically insulating silicide, which tends to dissociate at annealing temperatures of 360 °C and above. At thermodynamic equilibrium, the Au−Si system does not possess stable silicides. However, it was previously reported that crystalline silicides form at lower temperatures, whereas they dissociate into pure Au and Si phases at ∼400 °C.[32,33] To our knowledge, the electrical properties of the low-temperature silicides have not been reported. The second possibility is microvoid formation and their relaxation by the reflow of Au−Si eutectic melts. When atoms in crystalline Si diffuse into a thick film of

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Au, it is known that voids form because of the volume mismatch between the two phases.[34] We postulate that the voids can heal above the bulk eutectic temperature (~360 °C), where the collective motion of Au atoms can possibly backflow into the voids. This is in logical agreement with the fact that eutectic bonding requires an annealing temperature above eutectic and is often accompanied with pressure[23,35−38] even if Au−Si intermixing takes place at much lower temperatures. These explanations are somewhat speculative, but we hope that these arguments will stimulate future studies on the interface between Si and a thick Au film with an emphasis on the electrical properties.

Finally, the morphological evolution from regimes B to C to D with increasing temperature and annealing duration can be explained as Au dewetting from the Si surface accelerated by interdiffusion of Au and Si. It has been well-known that Au films on the Si surface are thermodynamically unstable and thus bead up to form individual islands.[39] For our transfer-printed Au films, however, a kinetic pathway must be provided to cause the Au film to rupture. Otherwise, the film morphology may stay smooth for prolonged periods of time even though the smooth pad is not thermodynamically stable. In the case of our Au films in regimes B−D, however, the interdiffusion of Au and Si at the interface causes local stress due to density mismatch, followed by mass flow of the Au−Si eutectic melt for stress relaxation. The interdiffusion and mass flow serve as a pumping mechanism for materials, which leads to roughened films in regime C and ultimately ruptured films in regime D. In summary, regime D is an ultimate stable morphology, whereas regimes B and C are quenched morphologies pinned by cooling to room temperature. Therefore, in order to fabricate a useful Au contact pad on Si by transfer printing, one must set the annealing temperature right above the eutectic melting and keep the annealing time short, followed by quenching to room temperature.

CONCLUSION

The electrical contact properties of transfer-printed Au films on Si substrates were explored as a function of the subsequent annealing conditions. Au−Si contact resistance values for the samples prepared with 12 different combinations of the annealing temperature and duration were measured using TLM, and their surface morphology alteration was examined. A transfer-printed Au film on Si exhibits significantly reduced contact resistance, comparable to that of vacuum-deposited Au on Si, when annealed at or above the bulk eutectic temperature. The surface of Au, however, roughens during the annealing process; thus, a controlled thermal treatment is required to fabricate useful metal−semiconductor contact using transfer printing. The drastic change of the contact resistance and surface morphology is attributed to the atomic-level mass transport between transfer-printed Au and Si, leading to their eutectic joining and Au dewetting. The findings in this work suggest that high-quality metal contact on the semiconductor can be realized via transfer-printing-based micromanufacturing, which complements conventional microfabrication.

ASSOCIATED CONTENT

Supporting Information

Experimental procedure, current−voltage (I−V) characteristics for poor electrical contact, and contact resistance between vacuum-deposited Au and Si. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Author

*E-mail: skm@illinois.edu.

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. H.K. and H.-J.C. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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